EUROPEAN PATENT APPLICATION

(54) **Zero temperature coefficient comparator circuit with hysteresis.**

(57) A single ended input comparator circuit (10) having an input inverter stage (16) and a voltage reference circuit is provided. The voltage reference circuit modulates the voltage appearing across the inverter stage thereby varying the switching threshold voltage level of the inverter stage and providing hysteresis for the comparator circuit. Further, by appropriately choosing the widths and lengths of the transistors used in the inverter stage and the voltage reference circuit, a zero temperature coefficient for the comparator circuit is achieved.
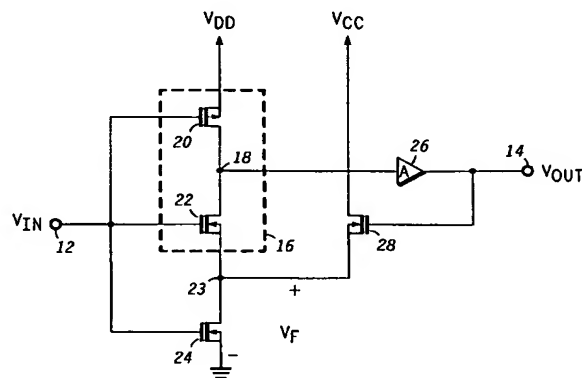
EP 0 551 742 A1

Field of the Invention

This invention relates to circuits and, in particular, to comparator circuits having hysteresis.

Background of the Invention

A comparator circuit with hysteresis is a comparator with two switching threshold levels; an upper switching voltage level and a lower switching voltage level wherein the upper voltage level is greater than the lower voltage level. In particular, if the previous output logic state of the comparator was a logic low, the comparator switches logic states when the input voltage exceeds the upper threshold voltage level. However, if the previous output logic state of the comparator was a logic high, the comparator switches logic states when the input voltage falls below the lower threshold voltage level. It is in this manner that hysteresis is achieved as is understood.

It is also desirable to provide a comparator with hysteresis whose switching voltage levels are independent of temperature. A typical circuit for providing a zero temperature coefficient comparator circuit with hysteresis is disclosed in a textbook entitled "Bipolar and MOS Analog Integrated Circuit Design" by Alan B. Grebene, John Wiley & Sons, 1984. In particular, figure 11.15 on page 559 shows a circuit for adjusting the voltage at the inverting input of the comparator by closing switch S_2 to short out resistor R_C in order to provide the lower switching threshold. However, this circuit includes a large number of devices, consumes a large die size area, and requires a current bias.

Hence, there exists a need for an improved zero temperature coefficient comparator circuit having hysteresis.

Summary of the Invention

Briefly, there is provided a comparator circuit having an input terminal and an output terminal, comprising an inverter circuit having an input and an output, the input of the inverter circuit being coupled to the input terminal of the comparator circuit, the inverter circuit being coupled to operate between a voltage appearing at a first supply terminal and a voltage appearing at a first circuit node; a voltage reference circuit being responsive to a logic signal appearing at the output terminal of the comparator circuit and being coupled between a second supply voltage terminal and the first circuit node for modulating the voltage appearing across the inverter circuit; and an amplifier circuit coupled between the output of said inverter circuit and the output terminal of the comparator circuit.

The present invention will be better understood from the following detailed description taken in conjunction with the accompanying drawing.

Brief Description of the Drawing

The sole figure is a partial schematic/block diagram of a zero temperature coefficient comparator circuit with hysteresis.

Detailed Description of the Drawing

Referring to the sole figure, there is illustrated a partial schematic/block diagram of comparator circuit 10 having input terminal 12 and output terminal 14. The comparator circuit includes inverter 16 having an input coupled to terminal 12 and an output which can be taken at circuit node 18. It is understood that inverter 16 forms the input stage of comparator circuit 10.

Inverter 16 includes PMOS transistor 20 and NMOS transistor 22 where PMOS transistor 20 has a source electrode coupled to a first supply voltage terminal at which the operating potential VDD is applied, and a gate electrode coupled to input terminal 12. The drain electrode of PMOS transistor 20 is coupled to the drain electrode of NMOS transistor 22 wherein the common drain electrodes form the output of inverter 16 at circuit node 18. The gate electrode of NMOS transistor 22 is coupled to input terminal 12, while the source electrode of NMOS transistor 22 is coupled to circuit node 23. The back gate electrodes of transistors 20 and 22 are respectively coupled to the source electrodes of transistors 20 and 22.

Transistors 24 and 28 provide the internal reference and hysteresis of comparator circuit 10. The drain electrode of NMOS transistor 24 is coupled to circuit node 23 and to the source electrode of NMOS transistor 28, while the gate electrode of NMOS transistor 24 is coupled to input terminal 12. The source electrode of NMOS transistor 24 is returned to ground. The drain electrode of NMOS transistor 28 is coupled to operating V_{CC}, while the gate electrode of the same is coupled to output terminal 14. Also, the back gate electrodes of transistors 24 and 28 are respectively coupled to the source electrodes of transistors 24 and 28.

In addition, amplifier 26 has an input coupled to circuit node 18, and an output coupled to output terminal 14. Also, voltage V_F is substantially equal to the voltage appearing at circuit node 23.

The switching threshold voltage level (trip point) of inverter 16, which is determined by the widths and lengths of transistors 20 and 22, are set to be a fraction of the voltage appearing across the source electrode of transistor 20 and the source electrode of transistor 22. Or equivalently, a frac-

tion of voltage difference between voltage V_{DD} and the voltage appearing at circuit node 23 (V_{23}). For example, the switching threshold voltage level of inverter 16 may be set to be the midpoint voltage between V_{DD} and V_{23} which can be expressed as (V_{DD} - V_{23})/2.

The present invention recognizes that by varying the voltage appearing at circuit node 23 (V_F), the switching threshold voltage level of inverter 16 can be correspondingly varied. As a result, upper and lower switching threshold voltage levels can be provided thereby providing hysteresis for comparator circuit 10.

Initially, assume a starting position of voltage V_{IN} being higher than upper input threshold voltage and voltage V_{OUT} correspondingly being a logic low voltage. In this case, NMOS transistor 28 will be rendered inoperative and the voltage at circuit node 23 will be substantially equal to zero volts. This sets inverter 16 to switch at a threshold level substantially equal to V_{DD}/2 which is known as the lower threshold voltage level (V_L). Therefore, as voltage V_{IN} falls below voltage V_L, inverter 16 switches and voltage V_{OUT} transitions from a logic low voltage level to a logic high voltage level thereby turning on NMOS transistor 28. Once transistor 28 turns on, transistors 28 and 24 form a voltage divider with respect to voltage V_{CC} which forces a predetermined voltage at circuit node 23 as denoted by voltage V_F. Thus, the voltage appearing at circuit node 23 has increased from substantially zero volts to voltage V_F wherein voltage V_F is determined by the size ratio of transistors 28 and 24. This now sets a new switching threshold voltage level for inverter 16 which is known as the upper threshold level (V_U). It is understood that because the voltage at circuit node 23 has increased, voltage V_U is greater than voltage V_L. As a result, hysteresis is achieved for comparator circuit 10 because now voltage V_{IN} must exceed voltage V_U (not voltage V_L) in order to cause the output of inverter 16 to switch from a logic high state to a logic low state.

Moreover, if voltage V_{IN} increases and exceeds voltage V_U, inverter 16 switches and voltage V_{OUT} transitions from a logic high voltage level to a logic low voltage level thereby turning off NMOS transistor 28. Once transistor 28 turns off, the voltage at circuit node 23 is substantially equal to zero volts and comparator circuit 10 is now set back to switch at its lower threshold voltage level (V_L) as aforedescribed.

It is worth noting that amplifier 26 substantially gains up the voltage occurring at circuit node 18 thereby holding the gate of NMOS transistor 28 to a high voltage (V_{DD}) when the voltage appearing at circuit node 18 is near voltage V_L.

In summary, the voltage appearing at circuit node 23 is modulated between a first voltage (ground reference) and a second voltage (V_F) to vary the switching threshold voltage level of inverter 16. This, in turn, provides the necessary hysteresis for comparator circuit 10.

A detailed analytical approach for determining voltages V_L, V_U and V_F is now presented.

Solving first for the lower trip point (V_L):

let $I_{DS(20)} = I_{DS(22)}$

Therefore, we obtain:

$$(W_{20}/L_{20})^*(k_p/2)^*(V_{DD}-V_{IN}-V_{Tp})^2 = (W_{22}/L_{22})^*(k_n/2)^*(V_{IN}-V_{Tn})^2$$

W_{20} and W_{22} are respectively the widths of transistors 20 and 22;

L_{20} and L_{22} are respectively the lengths of transistors 20 and 22;

V_{Tp} is the threshold voltage for PMOS transistor 20;

V_{Tn} is the threshold voltage for NMOS transistor 20; and

k_p and k_n are respectively the transconductance parameters for PMOS transistor 20 and NMOS transistor 22.

Now let $\beta = \{(W^{22}/W^{20})^*(L20/L22)^*(k_n/k_p)\}^{1/2}$
and $V_L = V_{IN}$

We then can obtain the following expression for V_L:

$$V_L = (V_{DD} - V_{Tp} + V_{Tn}^*\beta)/(\beta+1) \qquad (1)$$

Similarly, solving for the upper trip point (V_U):
let $I_{DS20} = I_{DS22}$
Therefore, we obtain:

$$(W20/L20)^*(k_p/2)^*(V_{DD}-V_{IN}-V_{Tp})^2 = (W22/L22)^*(k_n/2)^*(V_{IN}-V_F-V_{Tn})^2$$

Again, let $\beta = \{(W22/W20)^*(L20/L22)^*(k_n/k_p)\}1/2$
and $V_U = V_{IN}$

We then can obtain the following expression for V_U:

$$V_U = (V_{DD} + \beta^*V_F - V_{Tp} + \beta^*V_{Tn})/(\beta+1) \qquad (2)$$

Notice that the hysteresis voltage (V_{HYS}) is the difference between the upper and lower switching threshold voltage levels and can be expressed as:

$$V_{HYS} = V_U - V_L = \beta^*V_F/(\beta+1)$$

The feedback voltage (V_F) is determined as follows:

By design $I_{DS28} \gg I_{DS20} = I_{DS22}$
and thus $I_{DS24} \approx I_{DS28}$
Therefore, we obtain:

$$(W24/L24)^*(k_n/2)^*(V_{IN} - V_{Tn})^2 = (W28/L28)^*(k_n/2)^*(V_{OUT} -V_F - V_{Tn})^2$$

Let $\alpha = \{W24/W28)^*(L28/L24)\}1/2$
and $V_{IN} = V_U$
Thus $V_U = \{V_{OUT} -V_F + V_{Tn}(\alpha-1)\}/\alpha$ (3)
Now, equating EQNS. (2) and (3), we obtain:

$$(V_{DD} + \beta^*V_F - V_{Tp} + \beta^*V_{Tn})/(\beta + 1) = \{V_{OUT} -V_F + V_{Tn}(\alpha-1)\}/\alpha$$

Further, for $V_{IN} = V_U + \epsilon$ (where ϵ is some small but finite voltage and, thus, voltage V_{IN} is near the upper switching threshold voltage level), we obtain (due to amplifier 26) that $V_{OUT} \approx V_{DD}$.

Finally, we can obtain the following expression for V_F:

$$V_F = \{V_{DD}^*(1+\beta-\alpha)+V_{Tn}^*(\alpha- \beta- 1)+\alpha^*V_{Tp}/(\alpha^*\beta+\beta+1)\} \quad (4)$$

It should be realized that the terms k_n, k_p, V_{Tn} and V_{Tp} are sensitive to temperature variations. However, for a complementary MOS process wherein $V_{Tn} \approx V_{Tp}$, temperature variations can be eliminated by scaling the MOS transistors to appropriately select the values of α and β.

For example, let $V_{Tn} \approx V_{Tp}$
and by design establish $\alpha = \beta = 1$;
The following circuit characteristics are then obtained:

$V_L = V_{DD}/2$
$V_U = V_{DD}^*2/3$
$V_F = V_{DD}/3$
$V_{HYS} = Y_F/2 = V_{DD}/6$

From the above equations and analysis, it is clear that voltages Y_L, Y_U, Y_F, and V_{HYS} are all functions of voltage V_{DD} and are all independent of temperature under the assumption that voltage Y_{DD} is independent of temperature. Thus, a zero temperature coefficient comparator circuit with hysteresis has been provided.

By now it should be apparent from the foregoing discussion that a novel comparator circuit has been provided. The single ended input comparator circuit includes an input inverter stage and an internal voltage reference circuit. The internal voltage reference circuit modulates the voltage appearing across the inverter stage thereby varying the switching threshold voltage level of the inverter stage and providing hysteresis for the comparator circuit. Further, by appropriately choosing the widths and lengths of the transistors used in the inverter stage and the internal voltage reference circuit, a zero temperature coefficient for the comparator circuit is achieved.

While the invention has been described in conjunction with the specific embodiments thereof, it is evident that many alterations, modifications and variations will be apparent to those skilled in the art in the light of the foregoing description. Accordingly, it is intended to embrace all such alterations, modifications and variations in the appended claims.

Claims

1. A comparator circuit (10) having an input terminal (12) and an output terminal (14), comprising:
   an inverter circuit (16) having an input and an output, said input of said inverter circuit being coupled to the input terminal of the comparator circuit, said inverter circuit being coupled to operate between a voltage appearing at a first supply terminal and a voltage appearing at a first circuit node (23);
   a voltage reference circuit being responsive to a logic signal appearing at the output terminal of the comparator circuit and being coupled between a second supply voltage terminal and said first circuit node for modulating the voltage appearing across said inverter circuit; and
   an amplifier circuit (26) coupled between said output of said inverter circuit and the output terminal of the comparator circuit.

2. The comparator circuit according to claim 1 wherein said voltage reference circuit includes:
   a first NMOS transistor (24) having a drain, source, gate and backgate electrodes, said drain electrode of said first NMOS transistor being coupled to said first circuit node, said gate electrode of said first NMOS transistor being coupled to the input terminal of the comparator circuit, and said source and backgate electrodes of said first NMOS transistor being coupled to a third supply voltage terminal; and
   a second NMOS transistor (28) having drain, source, gate and backgate electrodes, said drain electrode of said second NMOS transistor being coupled to said second supply voltage terminal, said gate electrode of said second NMOS transistor being coupled to the output terminal of the comparator circuit, and said source and backgate electrodes of said second NMOS transistors being coupled to said first circuit node.

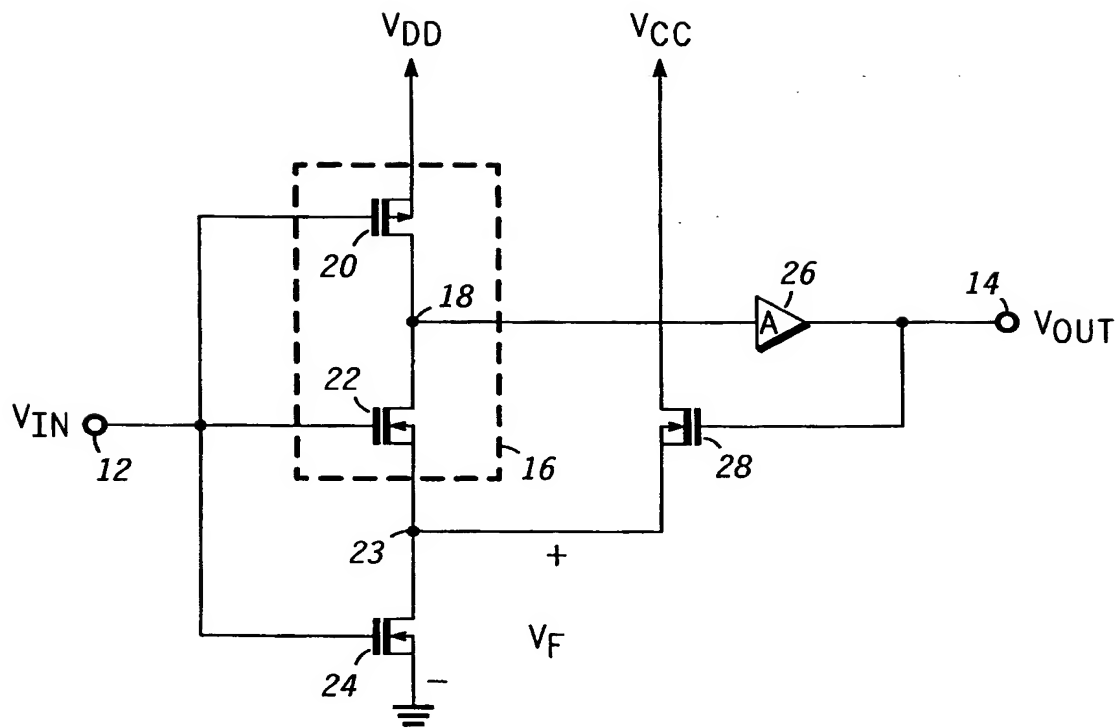3. The comparator circuit according to claim 2 wherein said inverter circuit includes:

a first PMOS transistor (20) having drain, source, gate and backgate electrodes, said source and backgate electrodes of said first PMOS transistor being coupled to said first supply voltage terminal, said gate electrode of said first PMOS transistor being coupled to said input of said inverter circuit, and said drain electrode of said first PMOS transistor being coupled to said output of said inverter circuit; and

a third NMOS (22) transistor having drain, source, gate and backgate electrodes, said drain electrode of said third NMOS transistor being coupled to said drain electrode of said first PMOS transistor, said gate electrode of said third NMOS transistor being coupled to said input of said inverter circuit, said source and backgate electrodes of said third NMOS transistor being coupled to said first circuit node.

4. A method for providing a zero temperature coefficient comparator circuit (10) having hysteresis, the comparator circuit including an inverter input stage (16) and a voltage reference circuit wherein both the inverter input stage and the reference circuit includes a plurality of transistors, the method comprising the steps of:

(a) modulating a voltage appearing across the inverter input stage such that a switching threshold voltage level of said inverter input stage is varied; and

(b) selecting the widths and lengths of the transistors used in the inverter input stage and the voltage reference circuit such that said switching threshold voltage level of said inverter input stage is substantially independent of temperature.

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
X	EP-A-0 437 039 (TEXAS INSTRUMENTS INC.) * page 3, line 36 - page 4, line 21; figure 1 * * page 6, line 10 - line 14; figure 7 * ---	1	H03K3/353
X	EP-A-0 316 884 (FUJITSU) * page 6, column 7, line 10 - column 8, line 15; figure 5 * ---	1	
X	PATENT ABSTRACTS OF JAPAN vol. 8, no. 272 (E-284)(1709) 13 December 1984 & JP-A-59 141 825 (MITSUBISHI) 14 August 1984 * abstract * ---	1	
A	EP-A-0 154 337 (TOSHIBA) * page 9, line 5 - page 10, line 25; figures 3,4 *	1,4	
	-----		**TECHNICAL FIELDS SEARCHED (Int. Cl.5)** H03K

The present search report has been drawn up for all claims		
Place of search THE HAGUE	Date of completion of the search 23 APRIL 1993	Examiner BUTLER N.A.

THIS PAGE BLANK (USPTO)